

FIG. 1

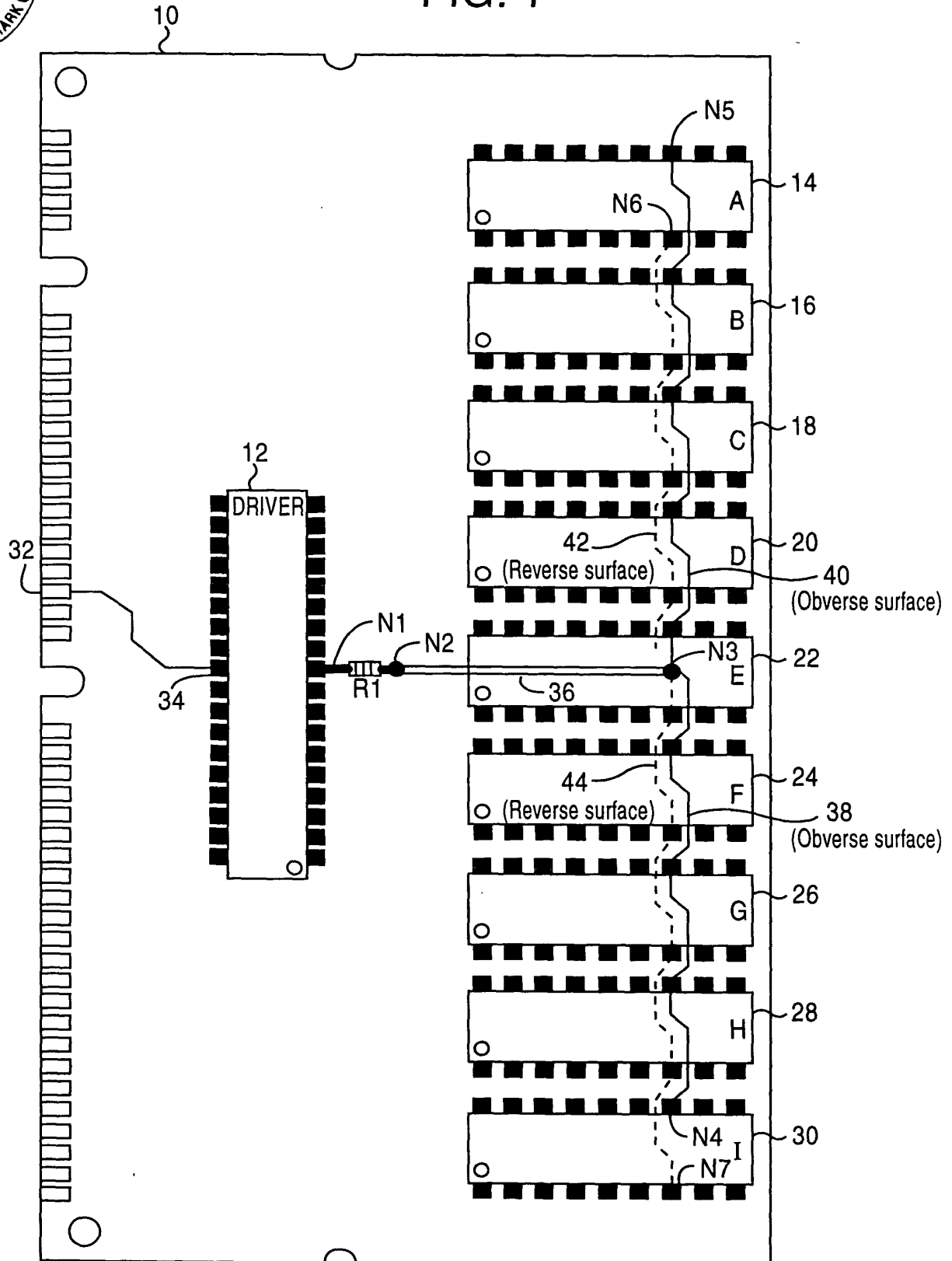




FIG. 2

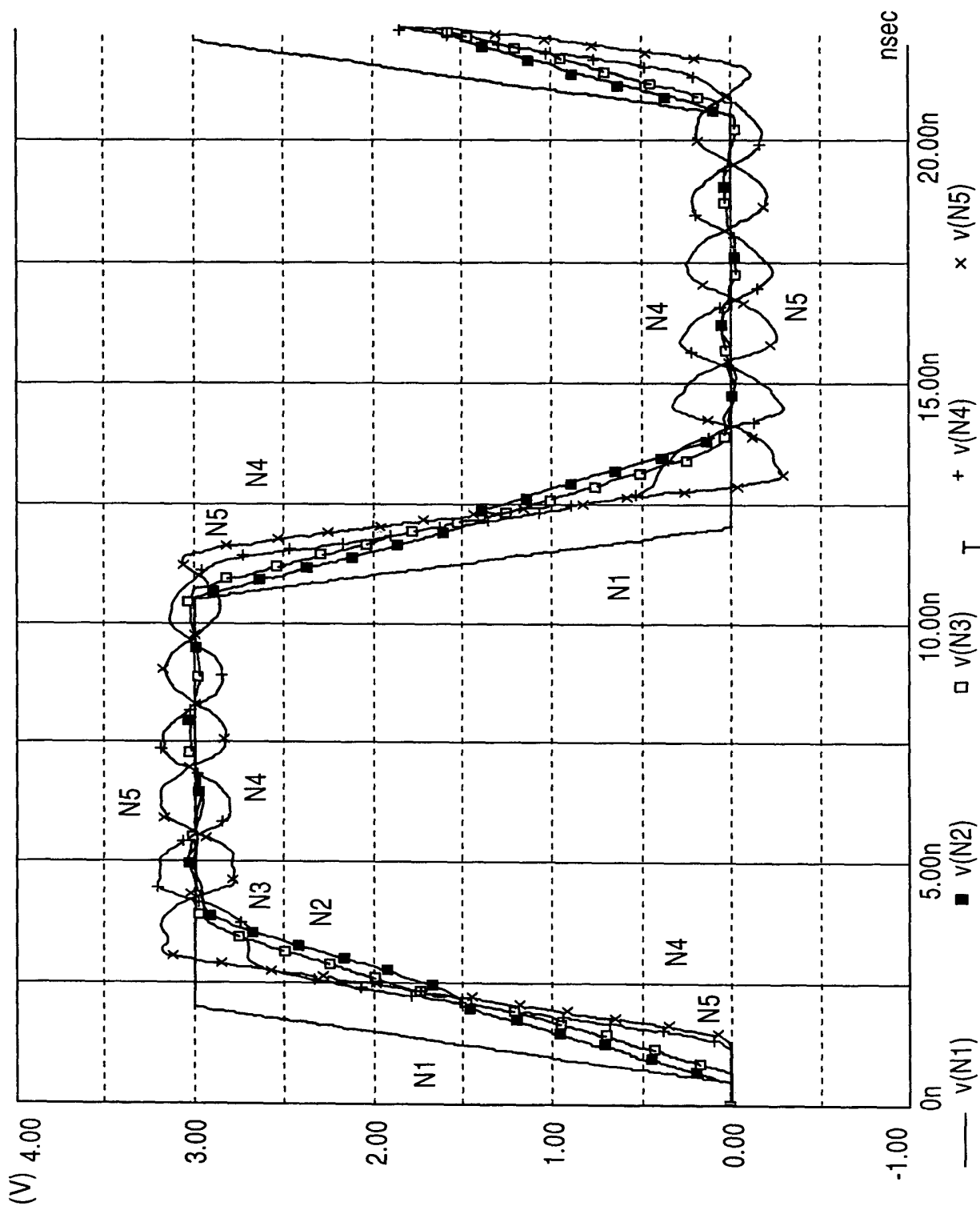




FIG. 3

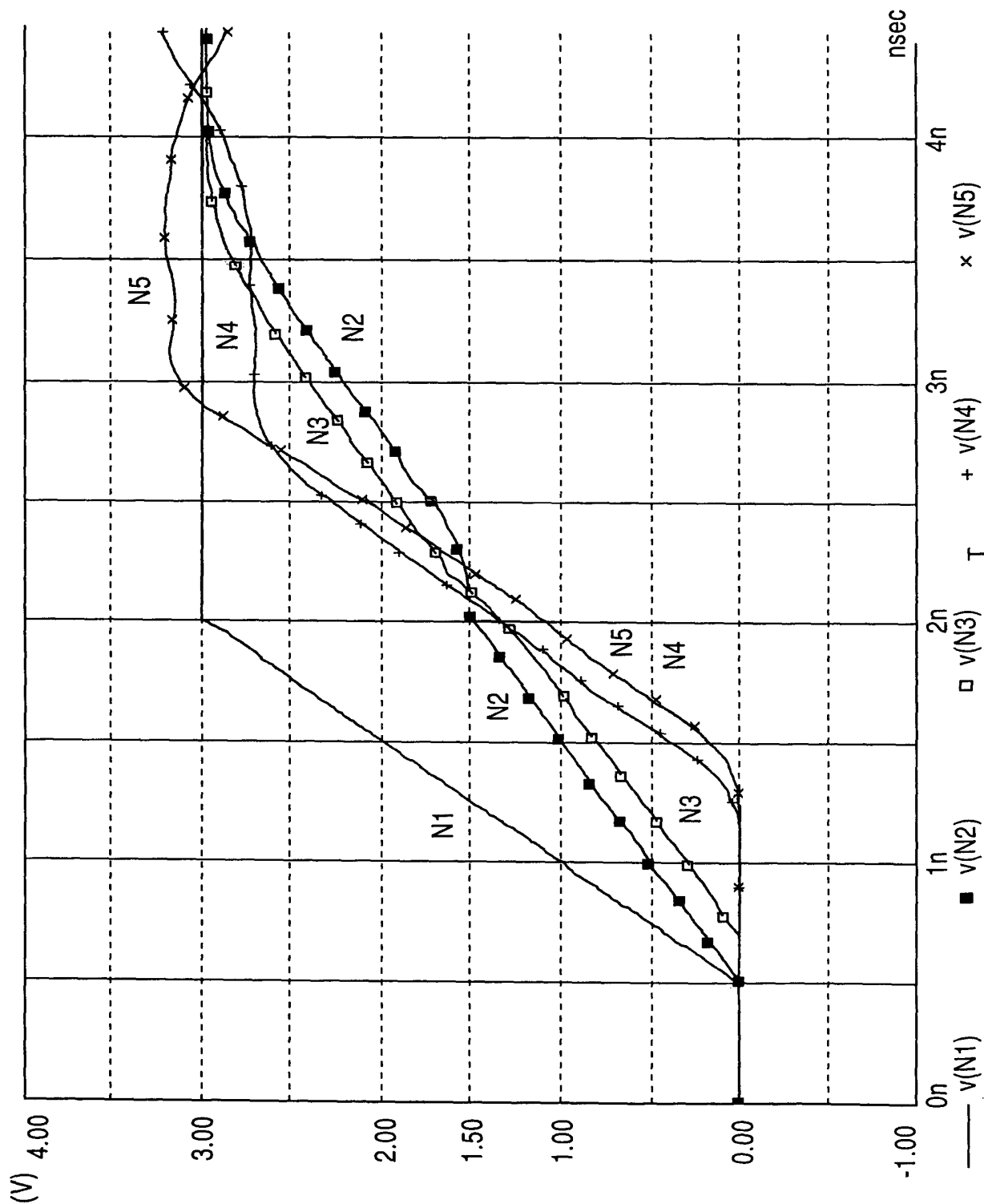
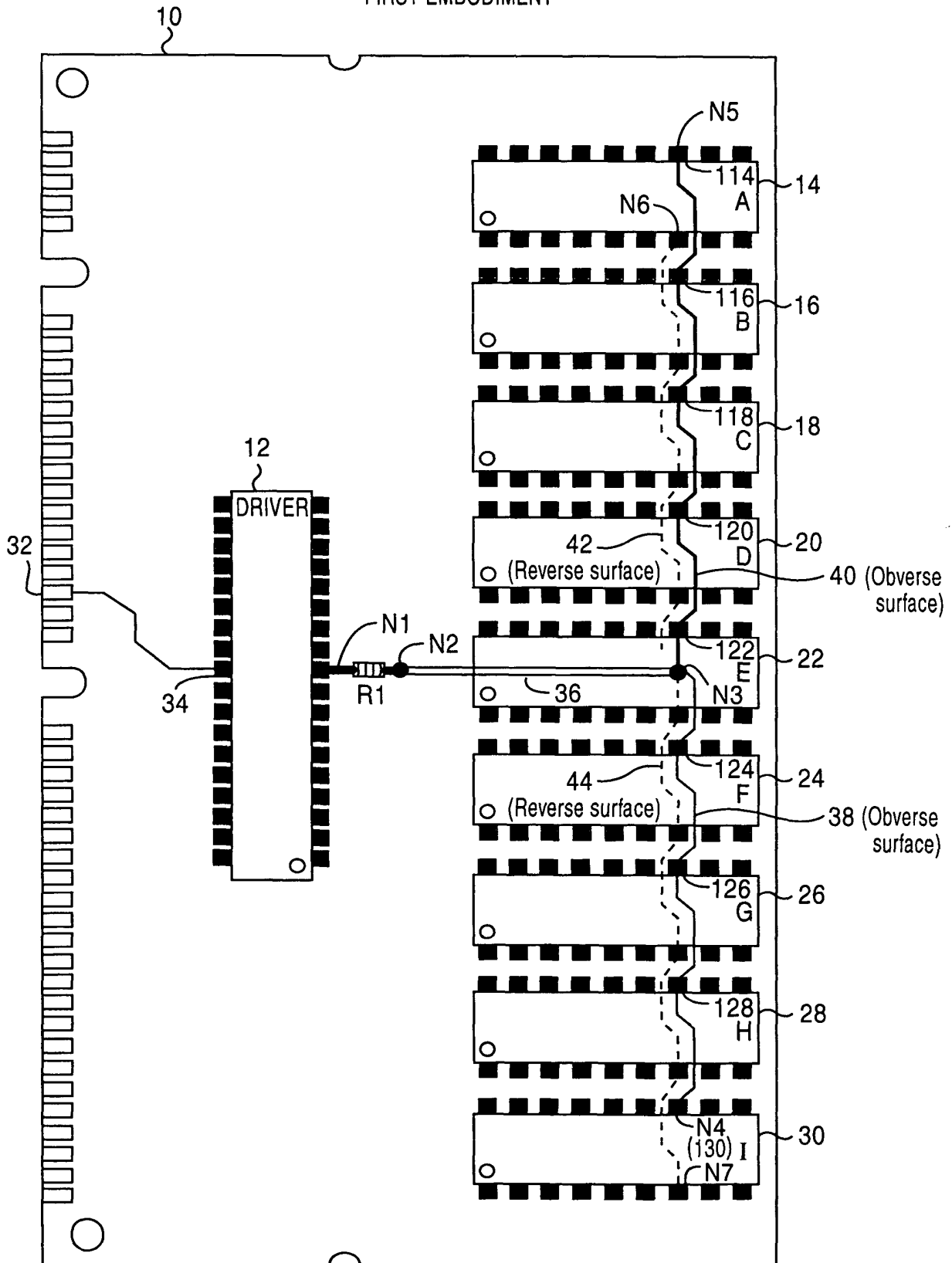


FIG. 4

## FIRST EMBODIMENT



$$Z_0 = \sqrt{\frac{L_0}{C_0 + C_d}}$$

or

$$=C114+C116+C118+C120+C122$$



## FIG. 6

### SIGNAL TRANSMISSION PERIOD TO WIDTHS FOR BRANCHED SIGNAL LINES

Width of branched signal line	Cd PF/m	Co PF/m	Lo nH/m	Zo $\Omega$	Td ns/m	Td1 ns/m
0.05 mm	250	71	520	85.6	6.08	12.92
0.10 mm	250	82	450	74.1	6.07	12.22
0.20 mm	250	109	356	57.1	6.23	11.31
0.40 mm	250	159	263	40.7	6.47	10.37
0.80 mm	250	252	173	26.2	6.60	9.32



FIG. 7

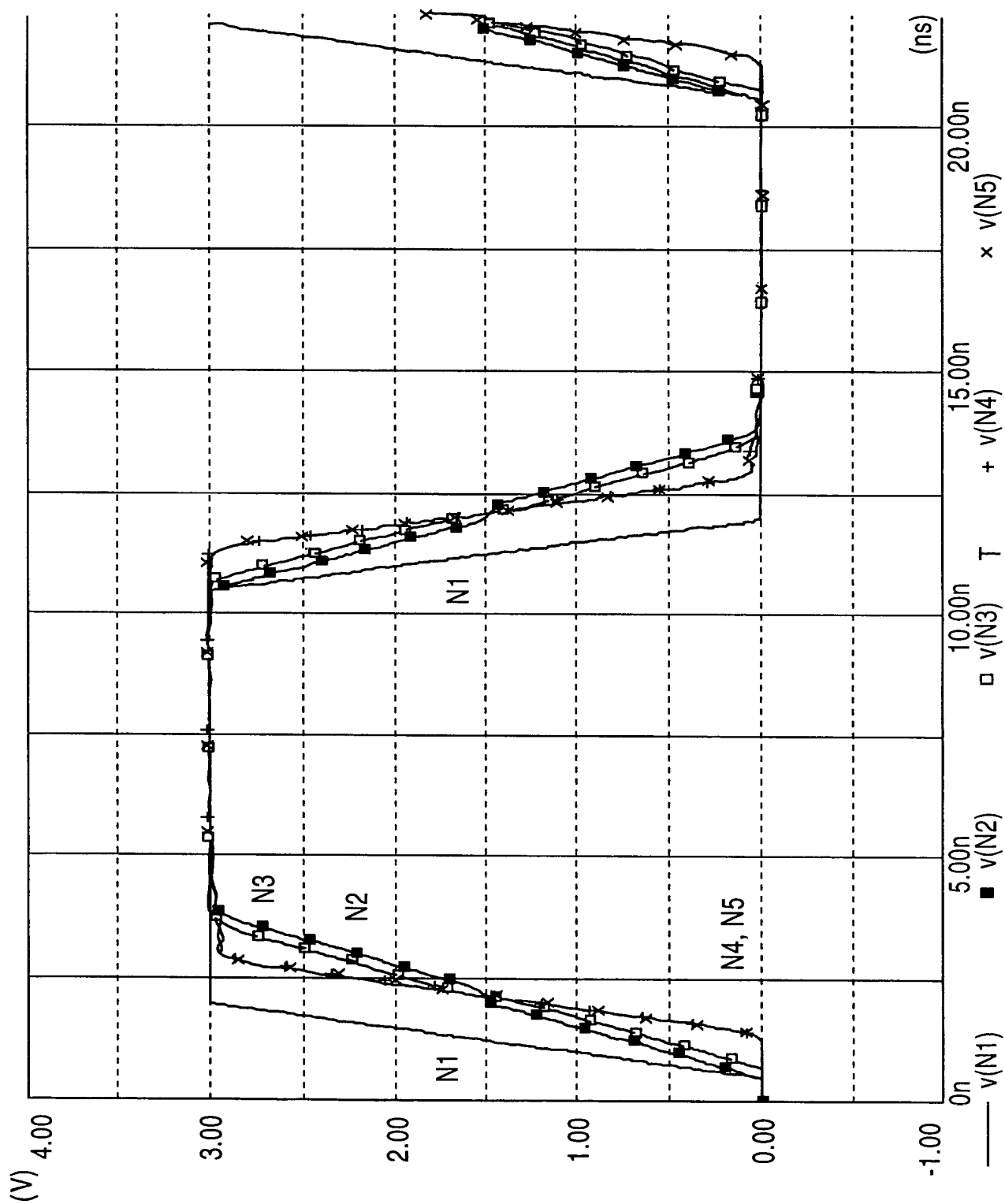
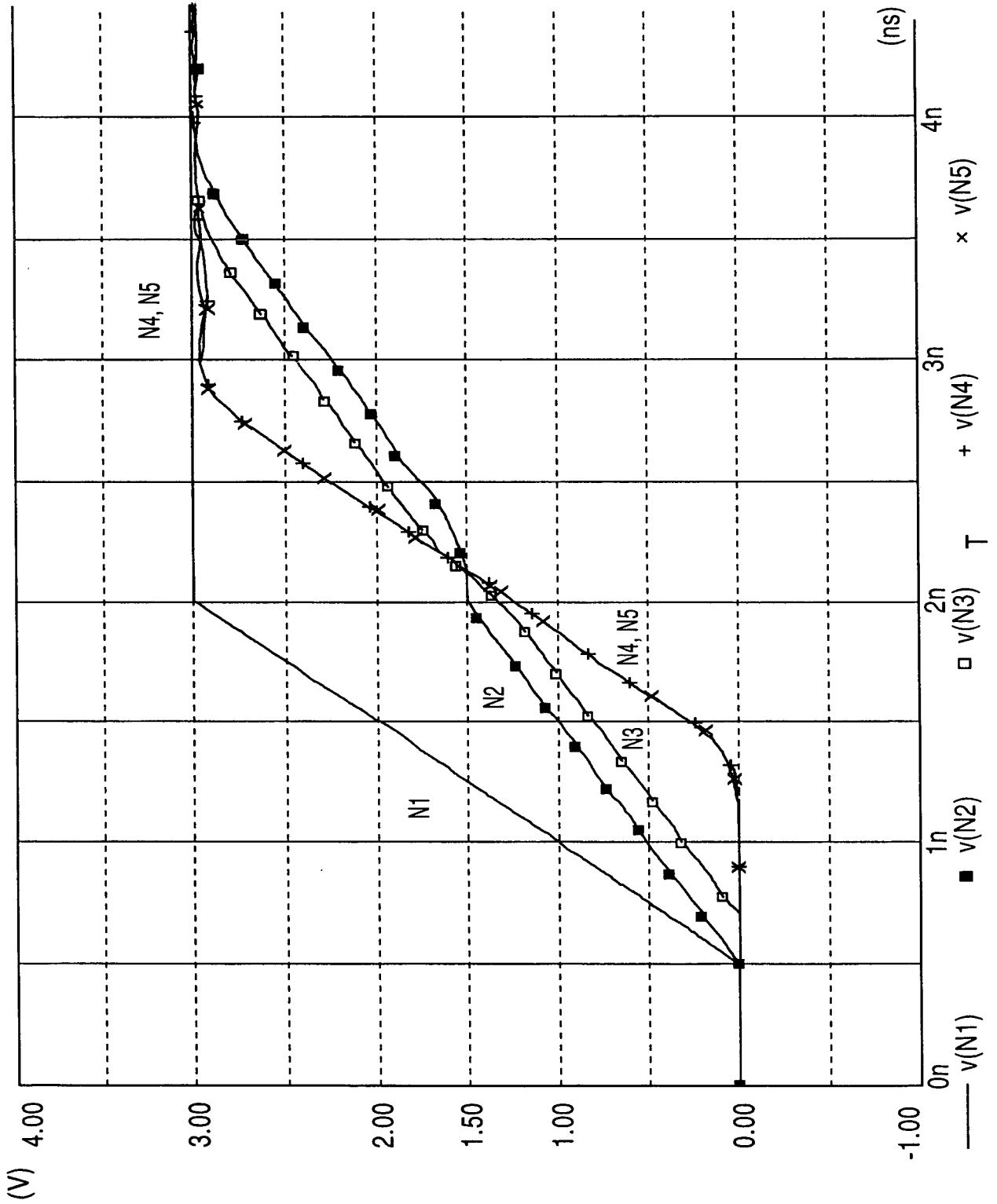
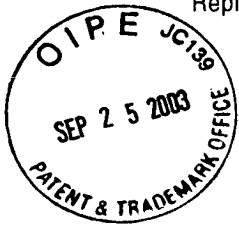




FIG. 8





**FIG. 9**  
 SECOND EMBODIMENT

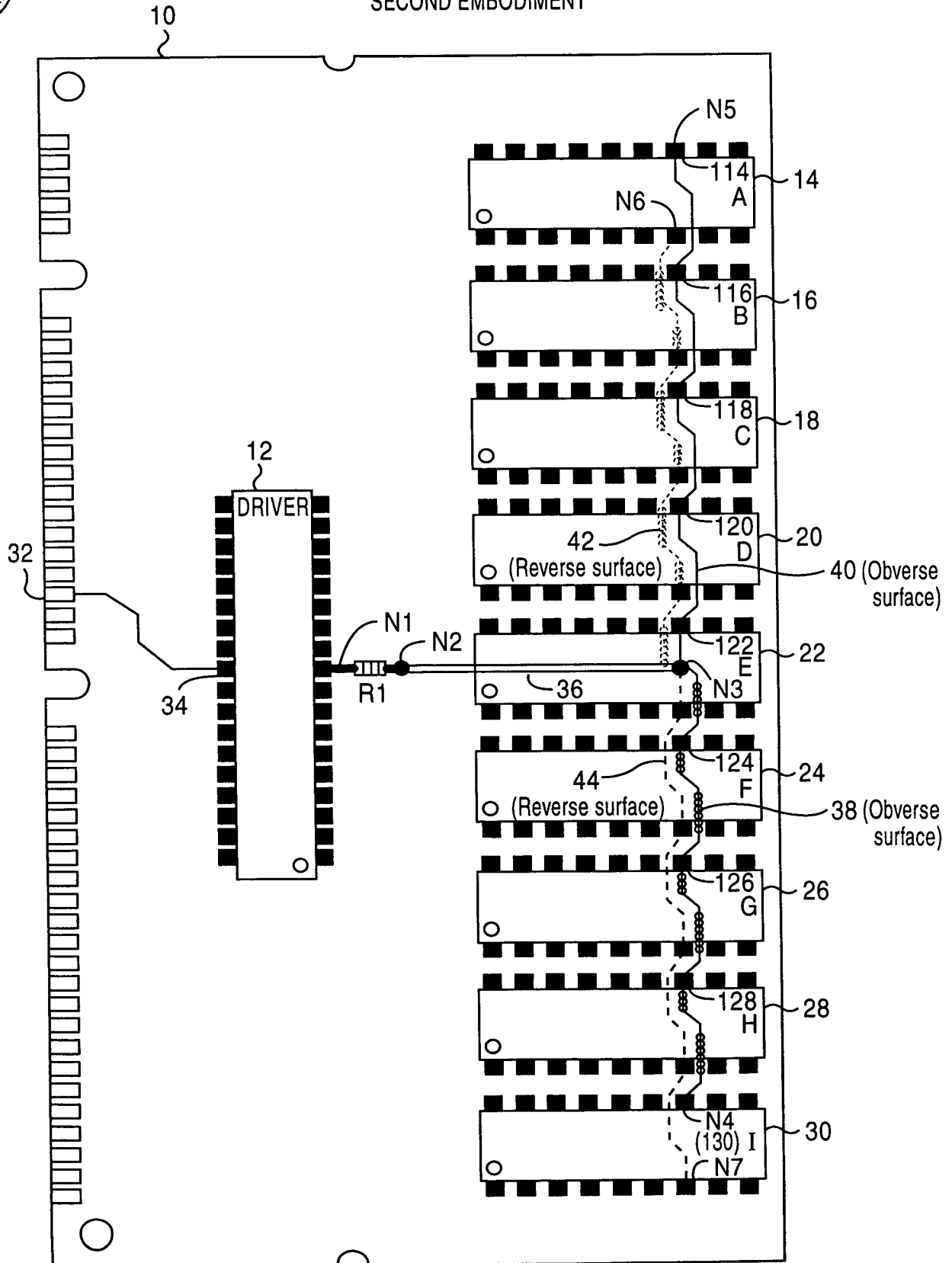




FIG. 10

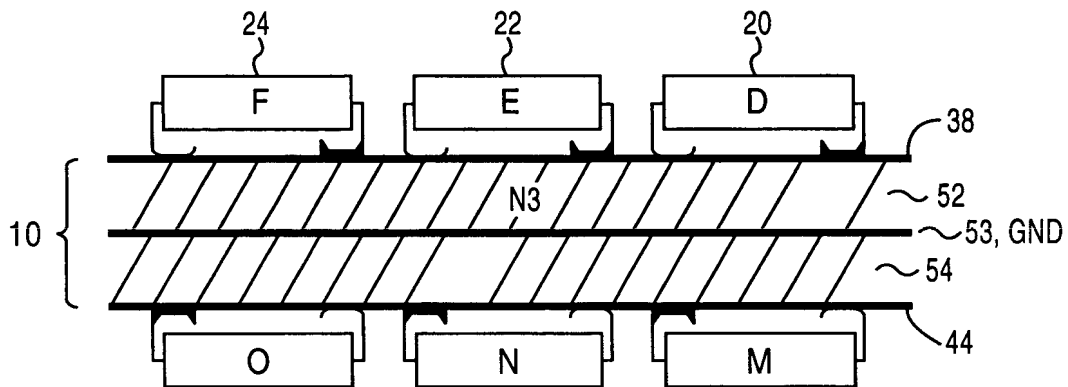


FIG. 11

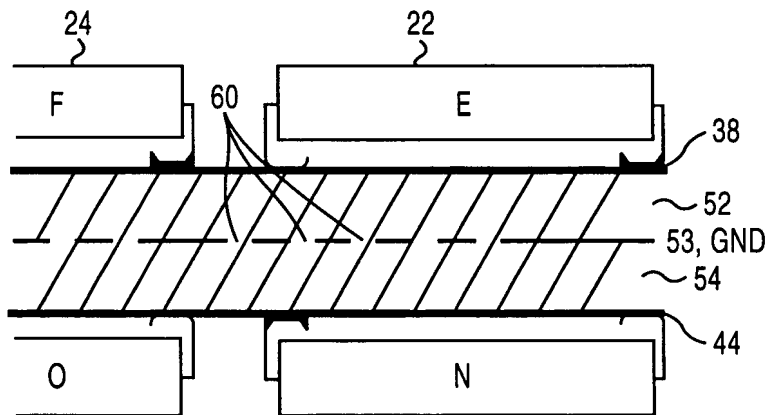




FIG. 12

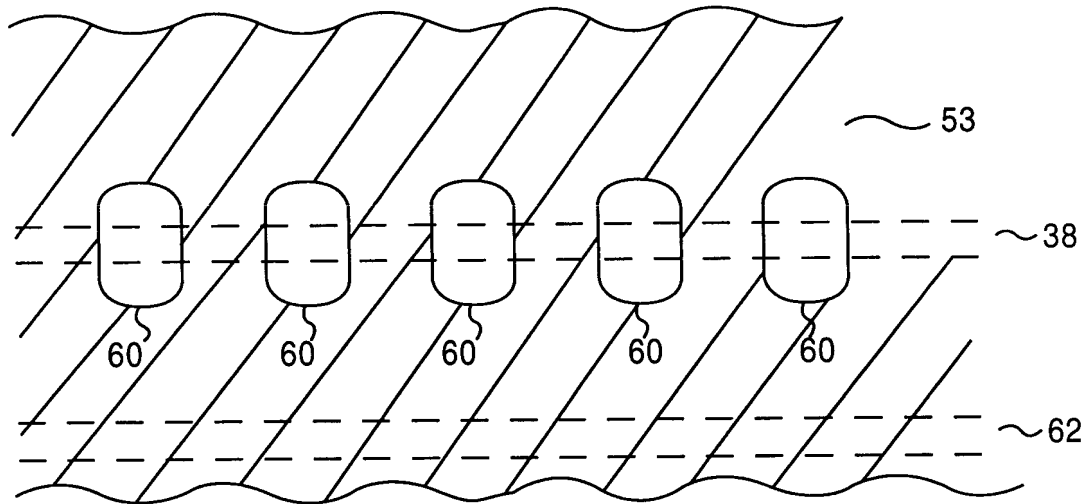


FIG. 13

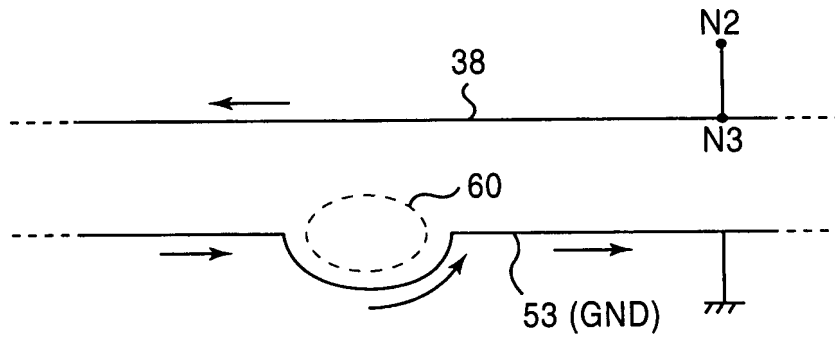


FIG. 4 is a schematic diagram of a fourth embodiment of the invention. It shows a circuit board 10 with a driver 12 and a series of nine modules A through I. The driver 12 is connected to a resistor R1, which is in turn connected to a series of nodes N1 through N7. Each module (A-I) contains a component (72a, 72b, 72c, 42, 36, 44, 70a, 70b) and is connected to the corresponding node. The modules are labeled with their obverse and reverse surfaces: 40 (Obverse surface) and 38 (Obverse surface).

## EQUIVALENT CIRCUIT FOR SIGNAL LINES

